



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,136	03/19/2004	Matthew F. Davis	8381/ETCH/SILICON/JB1	8916
55649	7590	03/12/2008		
MOSER IP LAW GROUP / APPLIED MATERIALS, INC. 1030 BROAD STREET 2ND FLOOR SHREWSBURY, NJ 07702				
EXAMINER				
ANGADI, MAKI A				
ART UNIT		PAPER NUMBER		
1792				
NOTIFICATION DATE		DELIVERY MODE		
03/12/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ATABOADA@MOSERIPLAW.COM
DOCKETING@MOSERIPLAW.COM



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/805,136
Filing Date: March 19, 2004
Appellant(s): DAVIS ET AL.

Alan Taboada
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/2/2008 appealing the Office action mailed 5/30/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,625,497	Fairbairn et al.	09-2003
2004/0078108	Choo et al.	04-2004
6,567,717	Krivokapic et al.	05-2003

2004/0087041	Perry et al.	05-2004
20030022510	Morgenstern	01-2003

(9) Grounds of Rejection

The following grounds of rejection are application to the appealed

(a) Claims 1-18 and 36-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fairbairn et al. (US 6,625,497) in view of Choo et al. (US 2004/0078108) and in further view of Krivokapic et al. (US 6,567,717) and Perry et al. (US 2004/0087041).

As to Claims 1, 15 and 36, Fairbairn et al. disclose a semiconductor processing module with integrated feedback/feed forward metrology, wherein a method of controlling a process of fabricating integrated devices is described, the method that includes: measuring a pre-etch dimension (CD) (column 4, line 42) and a post-etch CD (column 12, line 25) of at least one structure on a substrate. Adjusting a process recipe on an etch process (column 11, line 62) and enabling feedback to the photocell (lithography) (column 5, line 53) (column 10, line 64) or possibly photoresist trimming or shrinking (column 13, line 44) which are a capabilities for adjusting a process recipe of a pre-etch process.

Fairbairn et al. disclose *"A method and apparatus for processing a semiconductor wafer to reduce CD variation feeds back information gathered*

during inspection of the wafer to a previously visited processing tool and feeds forward information to adjust the next process the wafer will undergo" (abstract).

It is noted that Fairbairn et al. are silent about the "next process" being post-etch process in particular.

The reference of Choo et al. describe a system and methodology for monitoring and controlling a semiconductor fabrication process. Measurements are taken in accordance with scatterometry-based techniques of repeating in circuit structures that evolve on a wafer as the wafer undergoes the fabrication process. The measurements can be employed to generate feed forward and/or feedback control data that can be utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to adapt the fabrication process (abstract). The measurements can be utilized to generate feed forward and/or feedback control data that can be utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to achieve desired results (e.g., critical dimensions within acceptable tolerances and/or mitigation of overlay) (page 1, paragraph 0005). If not, one or more fabrication components and operating parameters associated therewith can be adapted accordingly based upon feedback/feed forward control data derived from the measurements. In one case, the measurement could be performed after trench etch. For instance, the volume, degree of abrasiveness and locations of slurry selectively distributed onto the wafer and/or the degree of pressure applied between a polishing pad and the wafer during a chemical

mechanical polishing (CMP) process can be adjusted to mitigate non-uniformity of the structure heights (page 5, paragraph 0042).

Choo et al. clearly teach measurement results (obtained after a given process step) can be used to forward-control any process step subsequent to the given step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. to extend the feed-forward information (obtained by measuring post-etch dimensions) to adjust the next process the wafer will undergo wherein the next process includes a post-etch process because Choo et al. teach feed-forward control based on wafer measurements. Choo et al. do not limit the nature of the initial process after which the measurement has been made nor do they limit which subsequent step is to be controlled, based on those measurements, suggesting that the method can be applied to any process thereby controlling any subsequent process. One of ordinary skill in the art would have been motivated to extend the feed-forward control of Fairbairn et al. to any post-etch process in order to correct deficiency from the lithography or the etch steps in later post-etch steps as taught by Choo et al. For example post-etch cleaning parameters can be adjusted if etched holes or trenches show abnormal amount of residues after the etch step.

Fairbairn et al., disclose measurement processes (col.12, lines 16-34) but are silent about a multi-pass process.

Krivokapic et al. disclose a semiconductor feed-forward control process wherein "non-conforming post-etch wafers may be returned for further etching if under-etched" (column 10, line 35), which in effect describes a multi-pass process when the under-etch is performed by design, for example when the etched layer thickness not well controlled.

The reference of Perry et al. disclose a control etch method based on an in-situ thickness measurement step.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. allowing an under-etched wafer to be re-processed or re-etched one or more than once as needed until the desired etch result is obtained which will make it a multi-pass process, the post-etched process of CD measurement will be repeated as well to compare results with a desired CD characteristics and to include the thickness measurement method of Perry et al. allowing wafers which are detected to be under-etched by a post-etch measurement step to be sent back to (or remain in) the etcher for additional etching with duration determined from the differential thickness between the measured etched depth and the target etch depth, or in the method of Fairbairn et al., the CD measurement can be compared to the target waveform, and if not matched, the wafer can be re-processed to match the desired profile. The process can be repeated more than once if necessary, because the methods of Krivokapic et al. and that of Perry et al. when combined with the method of Fairbairn et al. will result in further increase of yield and

decrease of production cost as initially suggest by Fairbairn et al. when discussing the benefits of feedback and feed-forward controls (column 13, line 8). One of ordinary skill in the art would have been motivated to include a multi-pass process to the control method of Fairbairn et al. in order to ensure process performance including the instance where some of the substrate parameters have been changed (e.g. previously deposited film quality), the controlled multi-pass method would be able to correct for such changes by automatic inspection and process adjustments.

As to Claim 3, it is noted that Fairbairn et al. are silent about detecting a failure; however, one of ordinary skill in the art would have been motivated to search and detect a failure of processing equipment, for instance, if the modified method of Fairbairn et al. yields post-etch CD measurements that are consistently out of specification. Equipment failure detection is a routine procedure when a process fault is detected, otherwise manufacturing yield will be greatly affected.

As to Claim 4, the reference of Fairbairn et al. discloses "Further exemplary embodiments of the present invention can be implemented. In these embodiments CD at the resist trim and feature etch processes (such as gate etch, shallow trench isolation (STI) trench etch, via etch, contact hole etch, metal etch, etc.) is tightly controlled using feedback and feed forward of CD

measurement in real time under controlled environmental conditions" (column 13, lines 14-22). As an example a typical dual-damascene via etch is performed on a substrate including a photoresist layer, a BARC layer, a low-k dielectric, and an etch stop layer. After the BARC open step, the substrate would consist of a photoresist featured layer and a film stack (photoresist and BARC) having at least a featured layer, and a low-k blanket layer, and a film stack (low-k and etch-stop layer) having at least one blanket layer.

As to *Claim 5*, the CD measurements suggested by Fairbairn et al., such as CD-SEM or optical inspection tool (column 4, line 58), are non-destructive measurements.

As to *Claim 8*, Fairbairn et al. discloses a CD measurement ex-situ to the etch chamber (Figure 9A-9C).

As to *Claims 9, 10 and 11*, a CD-SEM, as described by Fairbairn et al., measures topographic dimensions in the same processing system including the etch chamber (Figures 9A-C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al., willing to transfer the wafers out of the system, to perform the CD-SEM measurement (described by Fairbairn et al.) ex-situ in the case the CD-SEM is not integrated within the system, or move the wafers to the CD-SEM measuring

station if the station is available within the system as suggested by Fairbairn et al., because Fairbairn teaches the benefits of the measurement (Fairbairn et al. disclose external CD measurement is conventional in the art (column 2, line 40).

As to Claim 12, Fairbairn et al. describe in the “background art” section a method where the results of CD measurements are then used to adjust the etch recipe for the remaining wafers in the lot which is at least one subsequent substrate (column 3, line 6).

As to Claims 53 and 13, one pre-etch process is considered to be the photo cell exposure in the method of Fairbairn et al. (column 4, line 60) performed before pre-etch dimension measurement.

As to Claim 14, the reference of Fairbairn et al. describes a etch process and post etch cleaning (911) process (column 4, line 48) which could be performed after measuring the post etch measurement.

As to Claim 16, the reference of Fairbairn et al. describes a processing system including an etch chamber and a CD measurement unit (figures 9A-9C).

As to Claim 17, the reference of Fairbairn et al. teaches an external CD measurement is conventional in the art (column 2, line 40).

As to Claims 6, 7 and 18, the reference to Fairbairn et al. is silent about a measuring step which is performed in-situ within the etch chamber, however, the reference teaches the benefit of performing etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

The reference of Perry et al. describes an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (Figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

As to Claim 37, it would be obvious to one of ordinary skill in the art to expect some kind of a failure if the target CD waveform or depth is not achieved

after the final inspection step . Detecting equipment failure would be the first obvious trouble-shooting step.

As to Claim 38, Fairbairn et al. disclose "Further exemplary embodiments of the present invention can be implemented". In these embodiments, CD at the resist trim and feature etch processes (such as gate etch, shallow trench isolation (STI) trench etch, via etch, contact hole etch, metal etch, etc.) is tightly controlled using feedback and feed forward of CD measurement in real time under controlled environmental conditions" (column 13, lines 14-22). As an example a typical dual-damascene via etch is performed on a substrate including a photoresist layer, a BARC layer, a low-k dielectric, and an etch stop layer. After the BARC open step, the substrate would consist of a photoresist featured layer and a film stack (photoresist and BARC) having at least a featured layer, and a low-k blanket layer, and a film stack (low-k and etch-stop layer) having at least one blanket layer.

As to Claim 39, none of the measurements cited in the references above are destructive.

As to Claims 40 and 41, the reference to Fairbairn et al. is silent about a measuring step which is performed in-situ within the etch chamber; however, the reference teaches the benefit of performing etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

Perry et al. describe an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (Figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

As to Claim 42, Fairbairn et al. disclose a CD measurement ex-situ to the etch chamber (Figure 9A-9C).

As to Claims 43-45, a CD-SEM, as described by Fairbairn et al., measures topographic dimensions in the same processing system including the etch chamber (figures 9A-C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al.,

willing to transfer the wafers out of the system, to perform the CD-SEM measurement (described by Fairbairn et al.) ex-situ in the case the CD-SEM is not integrated within the system, or move the wafers to the CD-SEM measuring station if the station is available within the system as suggested by Fairbairn et al., because Fairbairn et al. teach the benefits of the measurement (Fairbairn et al. disclose external CD measurement is conventional in the art (column 2, line 40).

As to Claim 46, Fairbairn et al. describe in the "background art" section a method where the results of CD measurements are then used to adjust the etch recipe for the remaining wafers in the lot which is at least one subsequent substrate (column 3, line 6).

As to Claim 47, one pre-etch process is considered to be the photo cell exposure in the method of Fairbairn et al. (column 4, line 60) performed before pre-etch dimension measurement

As to Claim 48, Fairbairn et al. describe a post etch cleaning (911) process (column 4, line 48) which could be performed after measuring the post etch measurement.

As to Claim 49, Fairbairn et al. disclose a semiconductor processing module with integrated feedback/feed forward metrology wherein a method of

controlling a process of fabricating integrated devices is described, the method comprises: measuring a pre-etch dimension (CD) (column 4, line 42) and a post-etch CD (column 12, line 25) of at least one structure on a substrate and adjusting a process recipe on an etch process (column 11, line 62) and enabling feedback to the photocell (lithography) (column 5, line 53) (column 10, line 64) or possibly photoresist trimming or shrinking (column 13, line 44) which are a capabilities for adjusting a process recipe of a pre-etch process.

Fairbairn et al. disclose "A method and apparatus for processing a semiconductor wafer to reduce CD variation feeds back information gathered during inspection of the wafer to a previously visited processing tool and feeds forward information to adjust the next process the wafer will undergo" (abstract). It is noted that Fairbairn et al. are silent about the "next process" being a post-etch process in particular.

The reference of Choo et al. describes a system and methodology for monitoring and controlling a semiconductor fabrication process. Measurements are taken in accordance with scatterometry-based techniques of repeating in circuit structures that evolve on a wafer as the wafer undergoes the fabrication process. The measurements can be employed to generate feed forward and/or feedback control data that can utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to adapt the fabrication process (abstract). The measurements can be utilized to generate feed forward and/or feedback control data that can utilized to selectively

adjust one or more fabrication components and/or operating parameters associated therewith to achieve desired results (e.g., critical dimensions within acceptable tolerances and/or mitigation of overlay) (page 1, paragraph 0005). If not, one or more fabrication components and operating parameters associated therewith can be adapted accordingly based upon feedback/feed forward control data derived from the measurements. In one case the measurement could be performed after trench etch. For instance, the volume, degree of abrasiveness and locations of slurry selectively distributed onto the wafer and/or the degree of pressure applied between a polishing pad and the wafer during a chemical mechanical polishing (CMP) process can be adjusted to mitigate non-uniformity of the structure heights (page 5, paragraph 0042).

Choo et al. clearly teach measurements results (obtained after a given process step) can be used to forward-control any process step subsequent to the given step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. to extend the feed-forward information (obtained by measuring post-etch dimensions) to adjust the next process the wafer will undergo wherein the next process includes a post-etch process because Choo et al. teaches feed-forward control based on wafer measurements. Choo et al. do not limit the nature of the initial process after which the measurement has been made nor does he limit which subsequent step to control, based on those measurements, suggesting that his method can be applied to any process thereby controlling any

subsequent process. One of ordinary skill in the art would have been motivated to extend the feed-forward control of Fairbairn et al. to any post-etch process in order to correct deficiency from the lithography or the etch steps in later post-etch steps as taught by Choo et al.. For example post-etch cleaning parameters can be adjusted if etched holes or trenches show abnormal amount of residues after the etch step.

As to Claim 50, see discussion for Claim 16 above.

As to Claim 51, Fairbairn et al. teach an external CD measurement is conventional in the art (column 2, line 40).

As to Claim 52, Fairbairn et al. are silent about a measuring step which is performed in-situ within the etch chamber; however, the reference teaches the benefit of performing etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

Perry et al. describe an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (Figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

(b) Claims 19-21 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) in view of Choo et al. (US 2004/0078108), Krivokapic et al. (US 6,567,717) and Perry et al. (US 2004/0087041) as applied to claim 1 above, and in further view of Morgenstern (US 2003/0022510)

Fairbairn et al. disclose a trench etch (column 13, lines 14-22), but fail to specifically disclose a trench capacitor.

The reference of Morgenstern (US 2003/0022510) teaches the formation of a capacitive trench structure with a polysilicon electrode layer, wherein the etch process is performed with an HBr and Cl₂ chemistry (page 2, paragraphs 0033-0035). The flow rate of HBr:Cl₂ is 45:135 or 1:3 (page 3, paragraph 0044).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al.

by including a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl₂ chemistry because the reference of Fairbairn et al. teach the disclosed control method is applicable to any structure. One of ordinary skill in the art would be motivated to apply the method of Fairbairn et al. to a capacitive structure in order to control the capacitance characteristics and values with a high precision from wafer-to-wafer in a manufacturing environment.

(10) Response to Arguments

(i) *With respect to Claims 1 and 36*, appellants' arguments on pages 5-6 of the reply asserting that the combined reference of Fairbairn et al. (US Patent No. 6,625,497) Choo et al. (US Pub. No. 2004/0078108), Krivokapic et al. (US Patent No. 6, 567,717) and Perry et al. (US Pub. No. 2004/0087041) fail to teach the limitation of *"multi-pass process"* as recited in claims are not convincing.

Fairbairn et al. disclose in some embodiments, post-etch processing, such as ash stripping, wet cleaning and/or further CD measurement, by the module before the wafer is returned to a cassette (abstract). Fairbairn et al. addresss the problem of CD control by reducing CD variation by feeding back information gathered during inspection of a wafer and feeding forward information to adjust the next process the inspected wafers will undergo. According to Fairbairn et al., the DC measurement, etch processing, and post-etch cleaning are performed at a single module in a controlled environment (col.4, lines 40-50). Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust at least one post-etch process such as cleaning and/or CD measurement or perform it at least one more time to insure the multi-pass process was successful, which reads on appellants' limitation of adjusting at least one post-etch process while forming the at least one structure.

Appellants' arguments that there is a hindsight reconstruction to assert the teachings of Krivokapic are not persuasive. The reference of Krivokapic et al. disclose an automated production system in which feed-forward means for feeding forward wafers to minimize tolerance errors of critical performance parameters in processing semiconductor wafers (col.3, lines 50-67 and col.4, lines 1-20). The prior art of Krivokapic et al. teach the feed-forward method which returns under-etched wafers to the etch chamber to be re-etched (col.10, lines 35-38) is in effect a *"multi-pass process"*.

Appellants' arguments on page of 5 of the reply asserting that the reference of Perry et al. fail teach or suggest executing a multi-pass process are again not convincing. The reference of Perry et al. teach a method of controlling a recess etch process which is performed more than once as needed until the desired etch results are obtained which makes it a multi-pass process as outlined in the block diagram shown in Fig.6B.

Appellants' similar arguments about the reference of Morgenstern are not persuasive. Morgenstern discloses a process to modify the planarization step and the recess etch step in order to arrive at a process that can be better

Art Unit: 1792

integrated (paragraph 0009) which involves the step monitoring the thickness of the polysilicon layer by interference spectrometry (paragraph 0025).

The inventions disclosed in the reference of Faibairn et al., Choo et al., Krivokapic et al., Perry et al, and Morgenstern involve steps which are inherently multi-pass processes to enhance production throughput or yield by utilizing information gathered during in-process inspection of the wafers.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Maki A Angadi/
Examiner, Art Unit 1792

Conferees:

/Kathryn L Gorgos/

Kathryn Gorgos

Nadine Norton
SPE, AU 1792

/Nadine G Norton/
Supervisory Patent Examiner, Art Unit 1792